ULTRA-LOW POWER, HIGH PERFORMANCE IMAGING SYSTEM-ON-A-CHIP with CMOS ACTIVE PIXEL SENSORS

by

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ACTIVE PIXEL SENSOR TECHNOLOGY

Active pixel sensor (APS) is a second generation solid-state sensor technology featuring with one or more transistors per sensor element

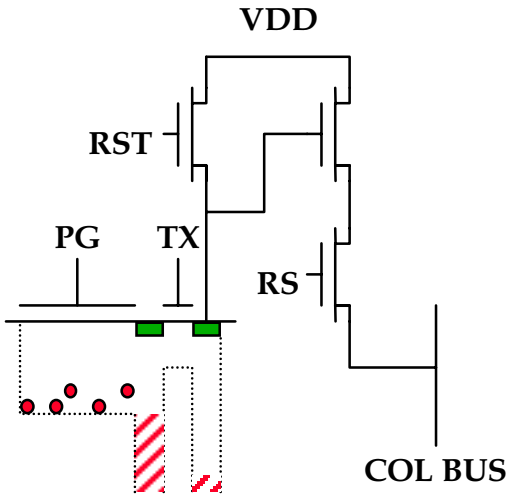
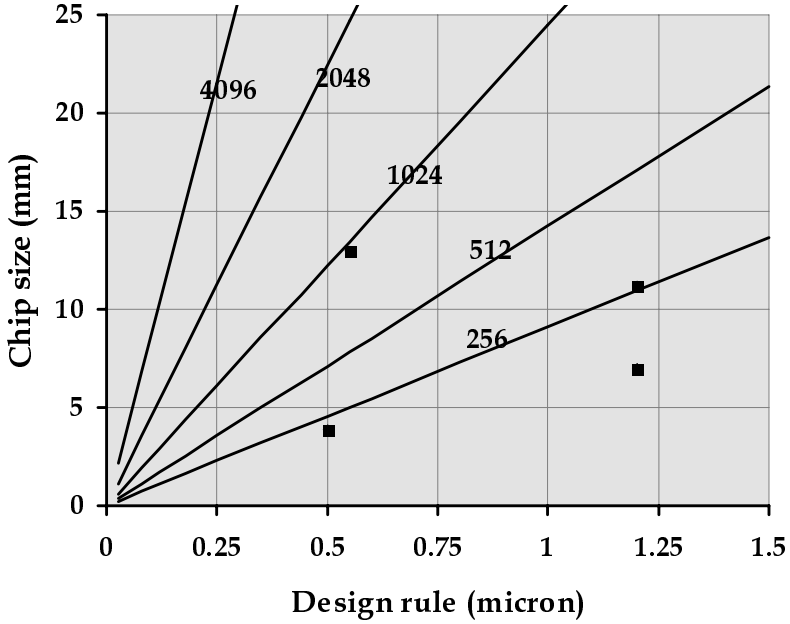


PHOTO-GATE (PG) APS

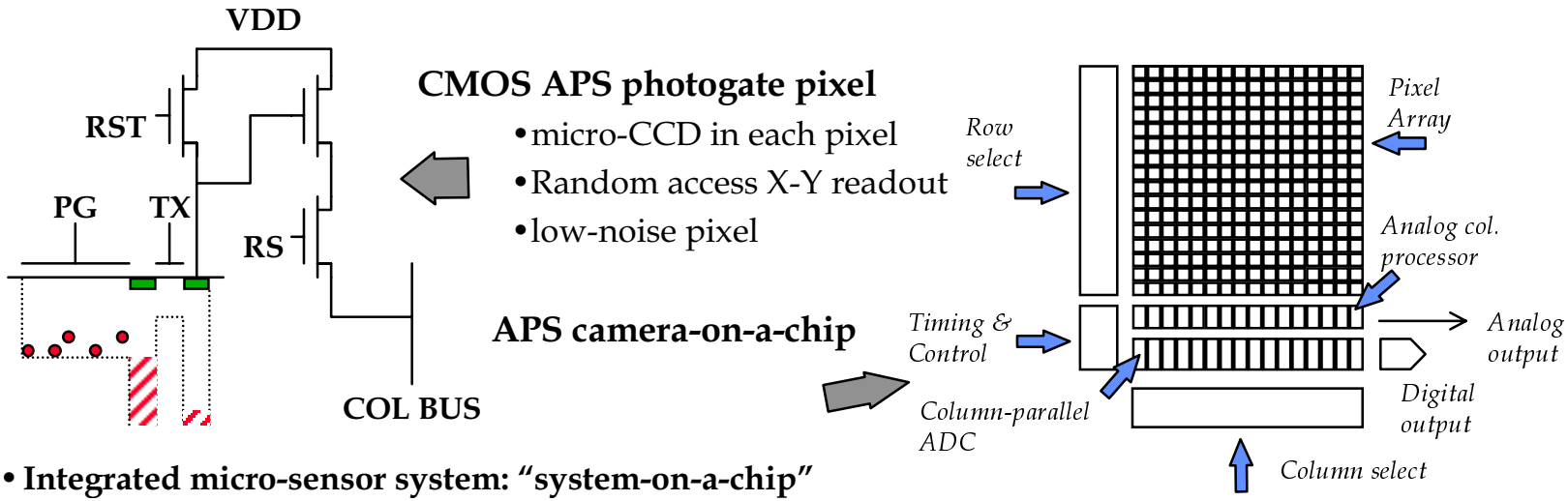


- *Integrate a micro-CCD in each pixel*
- *Use CCD detector for good QE*
- *Use buffer amplifier for low noise*
- *Use source-follower for high gain uniformity*
- *Use TX & RST gate as anti-blooming*
- *Random-access X-Y readout*

- CMOS APS made possible by continuously shrinking minimum feature size *(0.7x reduction per year)*
- Pixel size ~ 15 - 20 D (D is the design rule)

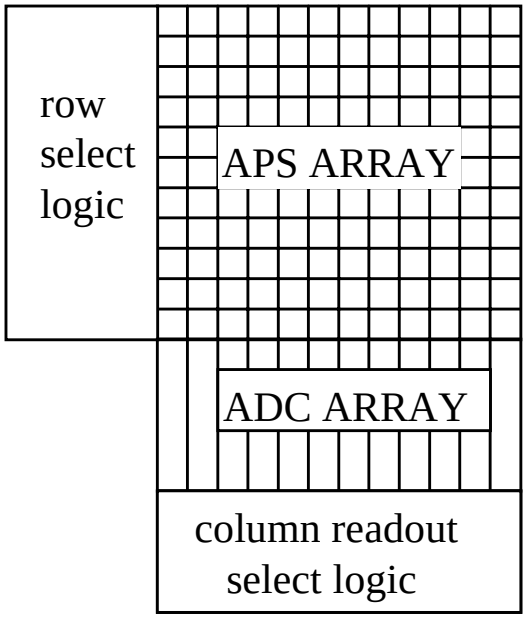
CMOS ACTIVE PIXEL SENSOR

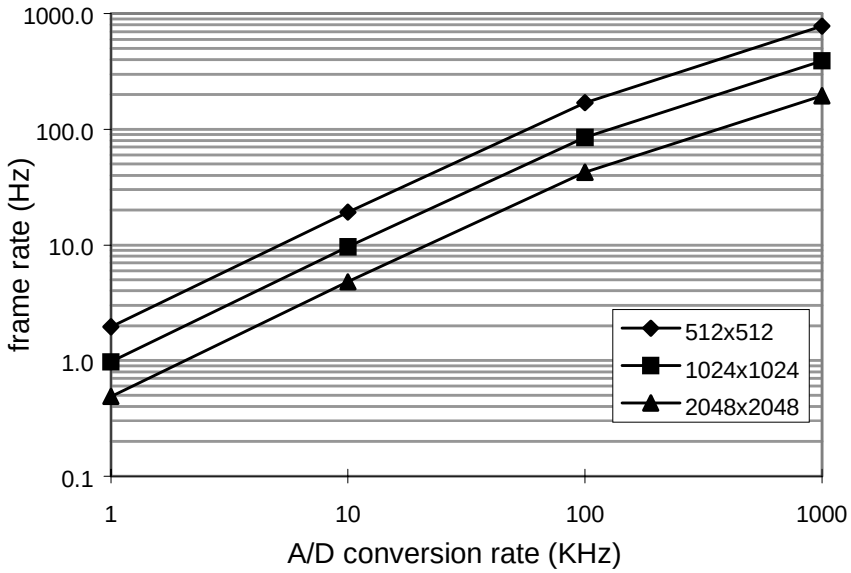
VERSATILE, HIGH-PERFORMANCE, LOW-POWER, INTEGRATED SENSOR TECHNOLOGY



- **Integrated micro-sensor system: "system-on-a-chip"**
  - –Enable miniaturization: 10x less mass and volume
  - –Simple digital interface; Standard power supply; Low chip pin count; More reliable
- **Excellent Image quality**
  - –comparable to CCD in noise, quantum efficiency, linearity, uniformity, dynamic range
- **Ultra-low power**: 100x less than state-of-the art
- **Multi-function multi-use:**
  - –Digital camera-on-a-chip; windowing; multi-resolution; High range; On-chip image processor
- **Large format, high resolution:** 1024x1024 with digital readout; small pixel size (10 µm)
- **High technology leverage:** Use CMOS technology
  - –Rapid scaling; Utilize advances in VLSI; Easy access; Low cost and fast delivery

COLUMN-PARALLEL FPA ADC





- ***Parallelism improves speed over serial analog readout***

Requirements:

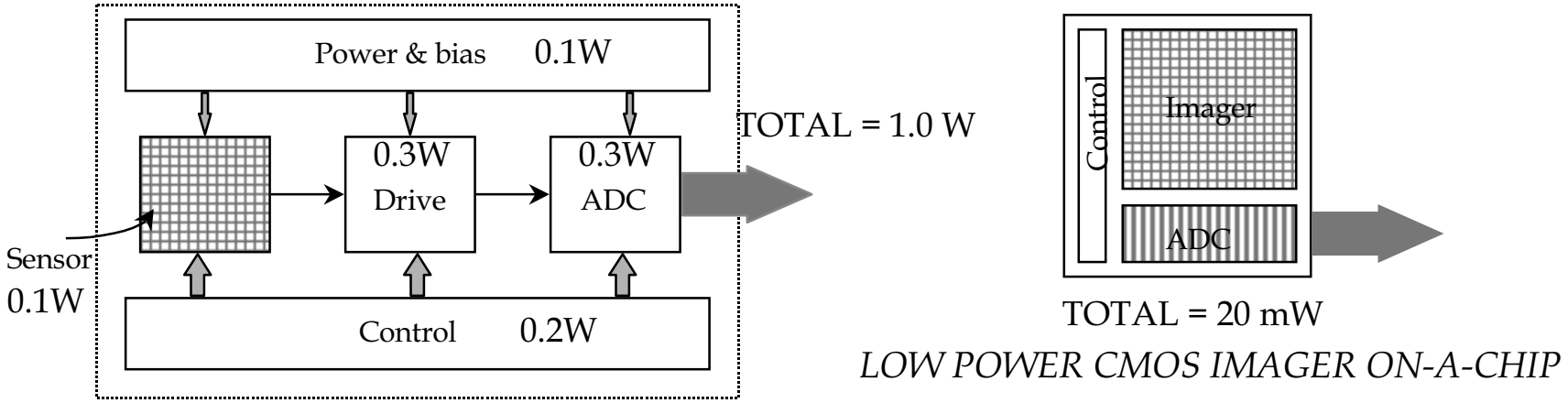
size: narrow pitch (10-20 µm); max. 5 mm ADC length

size requirement relaxed if ADC is multiplexed among multiple columns

low power: 50 to 150 µW/ADC; 0.1 - 1 µW/kHz

modest speed: 1K x 1K requires 33KHz minimum speed for 30 Hz frame rate

WHY IS CMOS APS LOW POWER



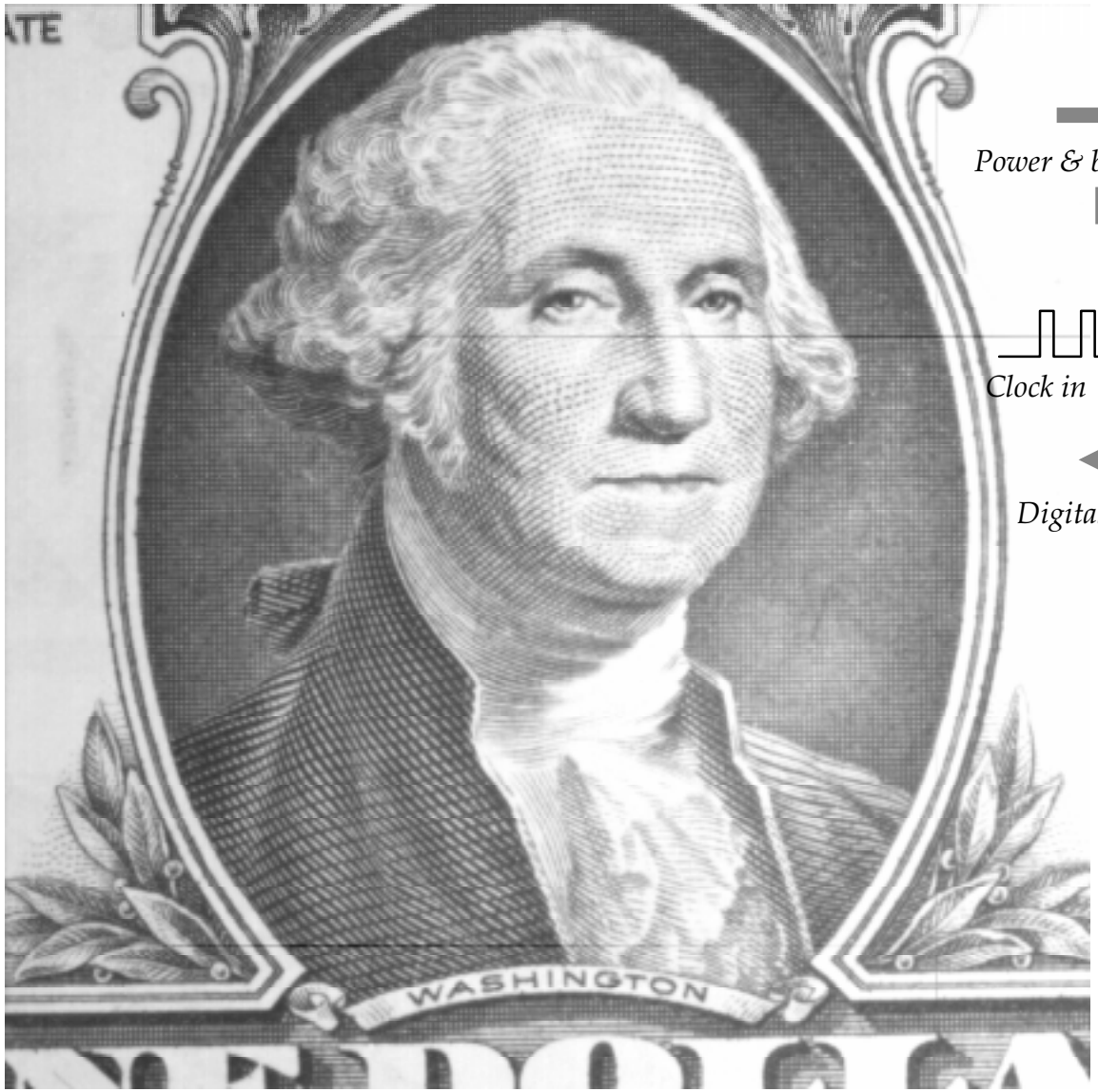
CONVENTIONAL IMAGER SYSTEM

LOW POWER CMOS IMAGER ON-A-CHIP

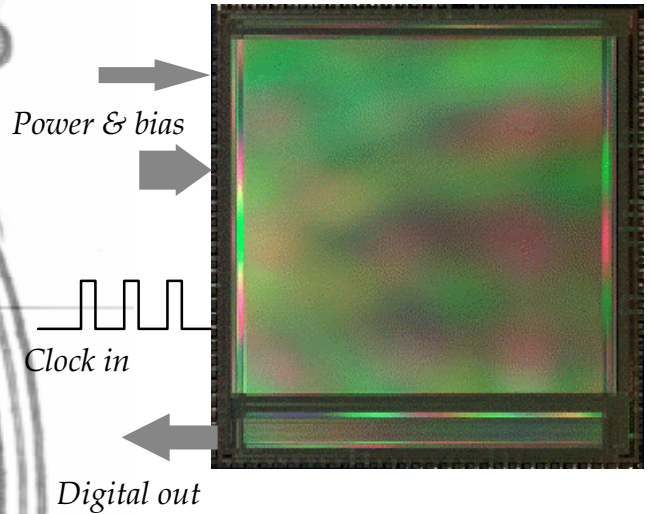
- Eliminates high power chip-to-chip communication
  - *no high speed analog communication (Power ~ frequency ^{2})*
  - *minimal large voltage swing digital I/O (Power ~ volt ^{2})*
- On-chip CMOS circuitry for timing & control enables ultra-low power
- Lower capacitance than CCD: leads to lower drive power
- Use of parallelism reduces power by eliminating parasitic loads

ON-CHIP INTEGRATION, SYSTEM MINIATURIZATION, LOW POWER GO HAND-IN-HAND

LARGE FORMAT CMOS APS



1K x 1K APS



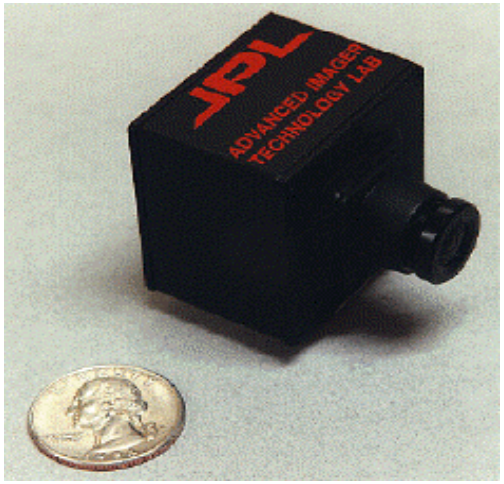
2.5 sec. exposure

- 1024x1024 format
- Pixel pitch: 11.9 µm
- **Digital output; no timing and control**
- Column-parallel single-slope **ADC**
- ADC resolution 10 bits
- Low power: 50 mW
- On-chip ramp-generator
- Needs off-chip bias

APS FEATURES & PERFORMANCE

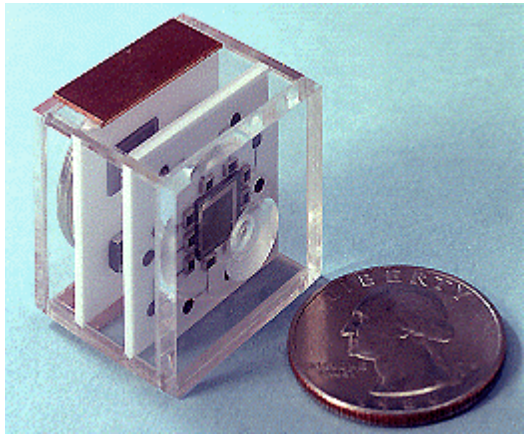
	Available	best results	near future
Array size	256x256	1024x0124	1024x1024
Pixel pitch (μm)	20	11	8
Technology (μm)	1.2; CMOS	0.6; CMOS	0.35; CMOS
Fill factor	25%	> 25%	10%
Peak QE: PG/PD	25%/60%	30%/60%	> 70%
Micro-optics	no	no	yes
Power supply	5V	3.3V	3.3V
Saturation	1.2V	1.0V	1.5V
Conversion gain (μV/e)	10	20	30
Noise (e^- r.m.s.)	13	5	<2
Dynamic range (dB)	76	80	120
Full well (e^-)	120,000	300,000	50,000
Dark current (pA/cm^2) @ RT	500	150	< 50
Speed (Mpix./sec.)	< 1	1	< 10
Power (mW/100kpix.)	3	3	< 2
Fixed pattern noise	< 0.1 % sat	< 0.1 % sat	< 0.1 % sat
Anti-blooming	yes	yes	yes
Windowing	yes	yes	yes
Rolling snap shutter	yes	yes	no
Snap-shot shutter	no	no	yes
On-chip timing	yes	no	yes
On-chip data compression	no	no	yes
Radiation hardness	1-10 krad.		> 100 krad.
On-chip ADC	no	yes	yes
ADC resolution (bits)		10	14
ADC power		1 μW/kHz	0.1 μW/kHz

MINIATURE APS CAMERA



Demonstration camera

- Computer serial interface
- Uses CC256 chip; **analog** sensor output
- Works on 5V supply
- Features user programmable windowing, exposure, panning
- Uses FPGA and ADC boards in addition
- Operable at 8-10 frames/sec.
- Low power



Mock-up of Wireless camera

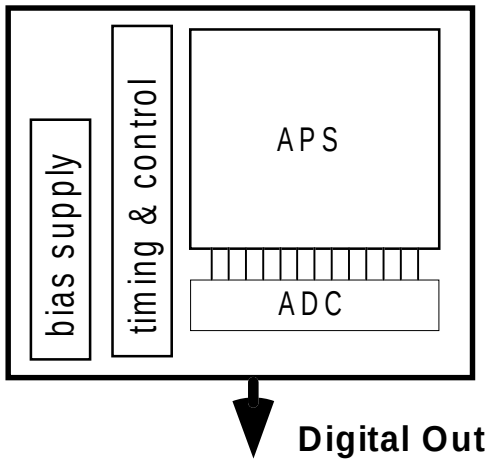
- Will use DICE chip; **digital** output
- Use off-the shelf comm. chips
- Dimensions: 1 inch cube
- Low power:

total RX/TX	~ 2 W
camera	~ 50 mW
sleep	~ 1.8 mW

- Transmit at 2.4 GHz
- Range: 1 k.m.; 2.5 Mbps rate

DIGITAL CAMERA-ON-A-CHIP

DICE CHIP



Requires only power, Gnd, Clock and one I/O

HIGH DEGREE OF FUNCTIONALITY

- **On-chip Timing and Control**
- **On-chip analog-to-digital converters (ADCs)**
- Supports Continuous or Digital Still Imaging
- Fully Programmable Exposure Time
- Programmable on-chip data reduction operations
  - Windowing (electronic panning)
  - Subsampling (electronic zooming)

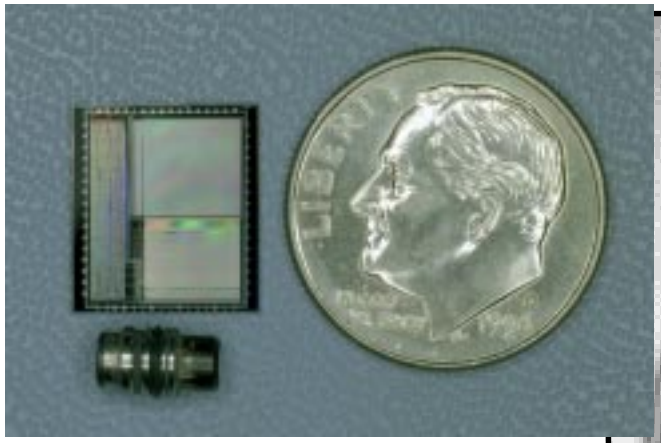
SIMPLE VERSATILE INTERFACE

- **Complete Digital Interface**
  - All analog references generated on-chip
  - Programmable with single wire
- Supports a variety of Digital Interfaces
  ex) Serial or parallel output

ULTRA LOW POWER

- Enters Low Power (mWatts) Idle mode after Digital Still
- Circuits turned off during imaging operation to reduce power

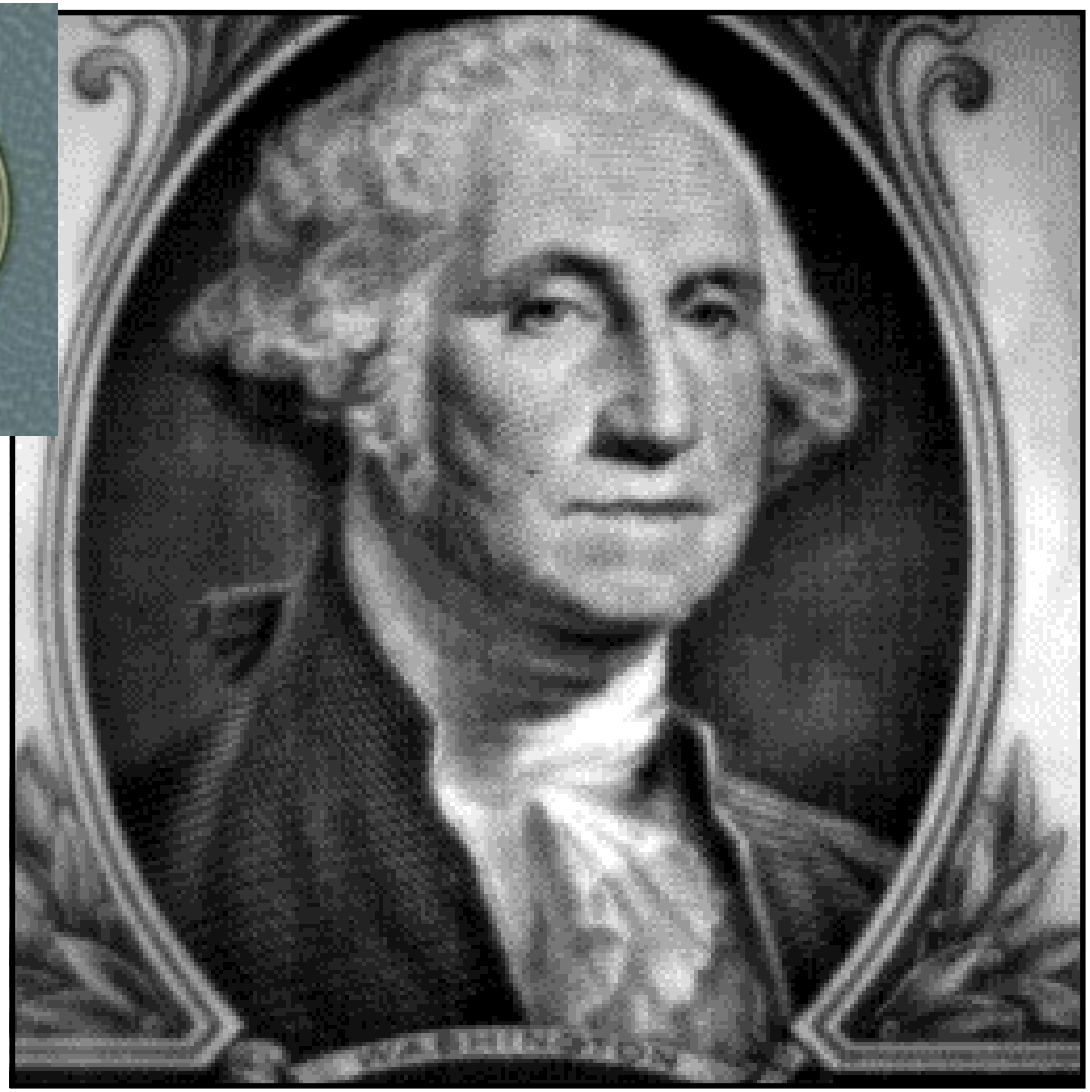
IMAGING PERFORMANCE



Chip picture

Features:

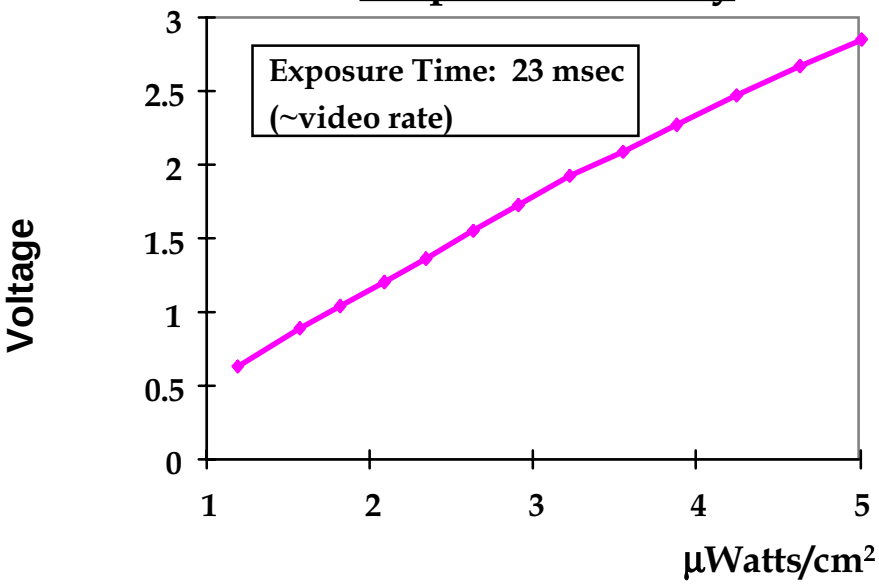
- Initially 256^2; designed for 1024^2;
- Chip size: 9.3 mm x 11.2 mm
- Ultra Low power:
  20 mW; 10 µW (standby)
- Max. data rate: 10 Mbits/sec.



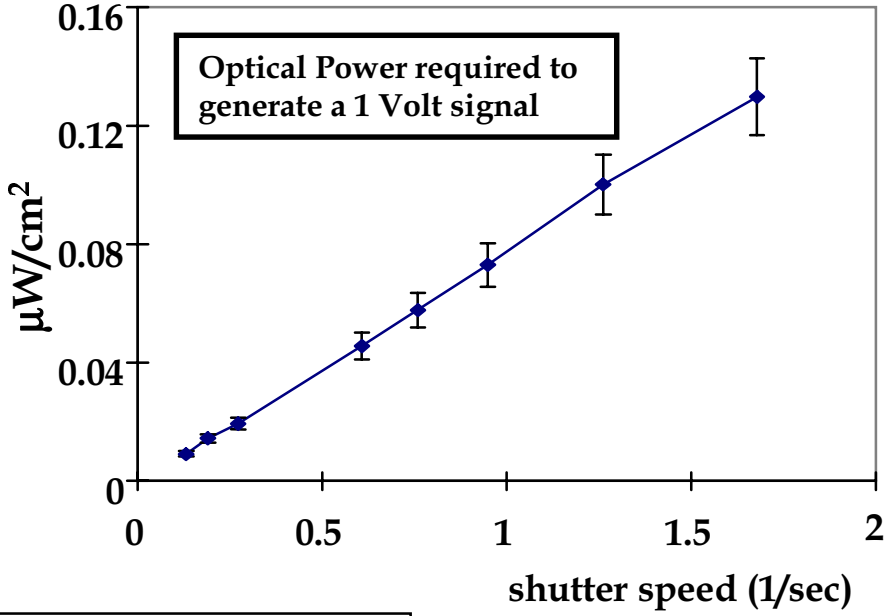
8 bit image from 256 x 256 DICE

IMAGER RESPONSIVITY

Response Linearity

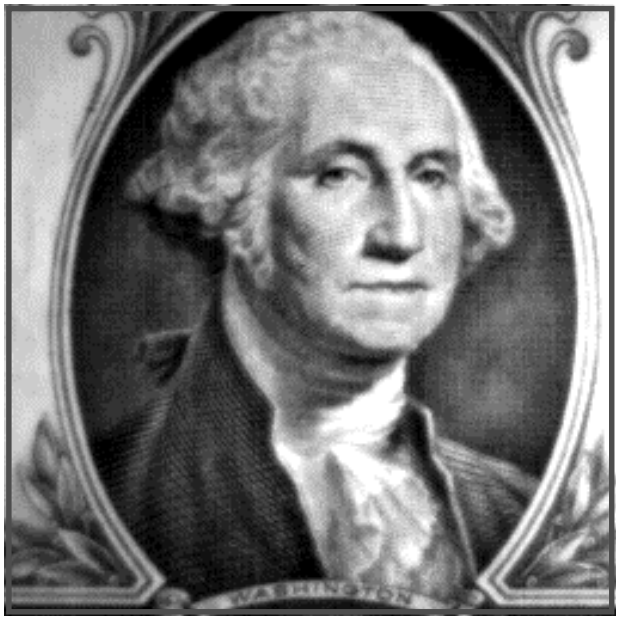


Exposure Programmability



SH time: 280 msec
ADC conversion time: 240 msec
TX: 1 Volt
VLN: 5.5 mA
ADC Range: 3 V
Clock: 500 KHz
Output data rate: 43 Kpix/sec (10 bit serial output)

ON-CHIP DATA REDUCTION

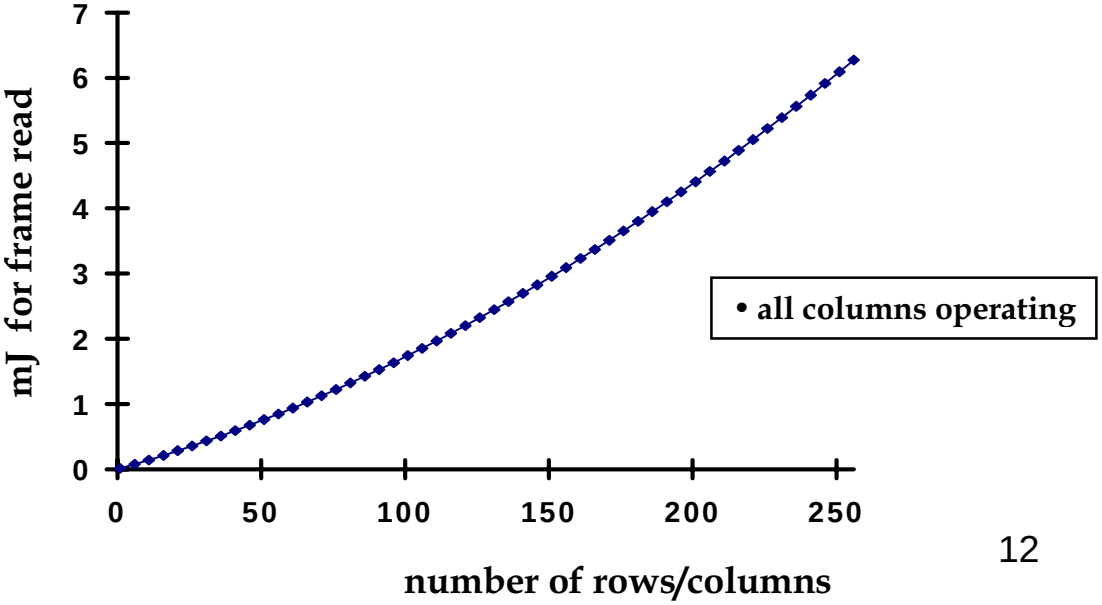


2.5 MHz clock
215 Kpixels/sec
VLN: 5.5 mA
TX: 1 Volt
ADC Range 2.4 V.
10 bits serial output

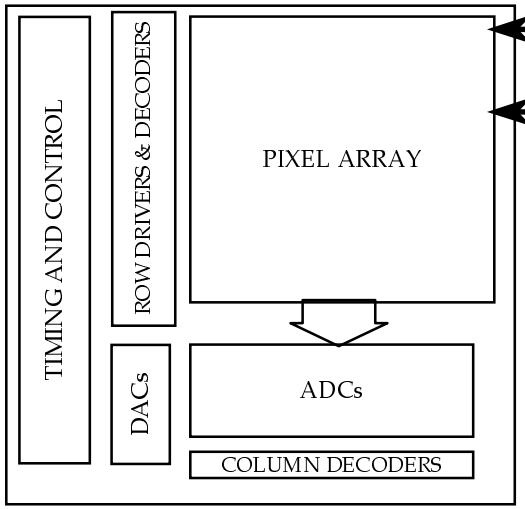
WINDOWING

SUBSAMPLING

(2 x 2 subsampling)



DICE SIGNAL CHAIN



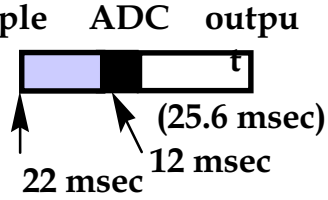
read pointer

integrate pointer

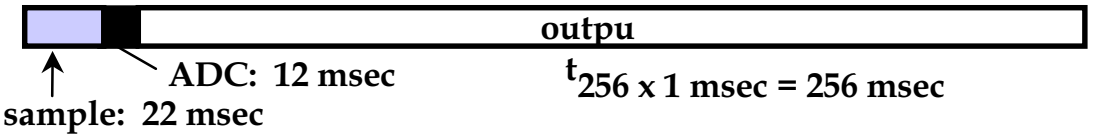
INTEGRATION TIME

Row Operations

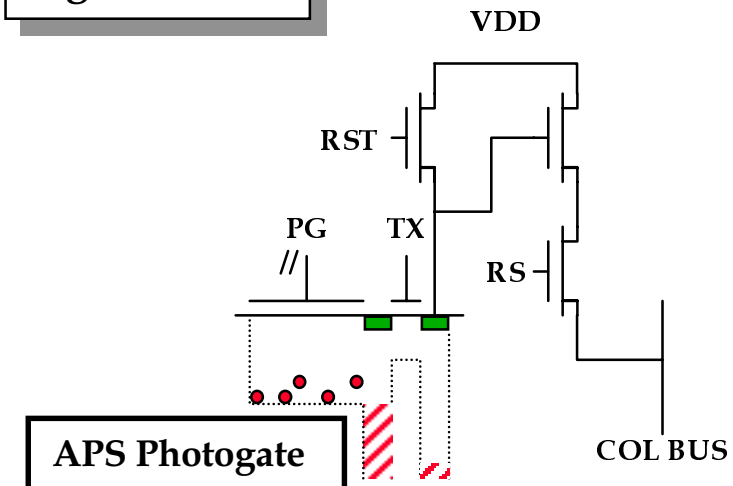
Parallel Output:
(4.3 Mpixels/sec)



Serial Output: (.9 Mpixels/sec)

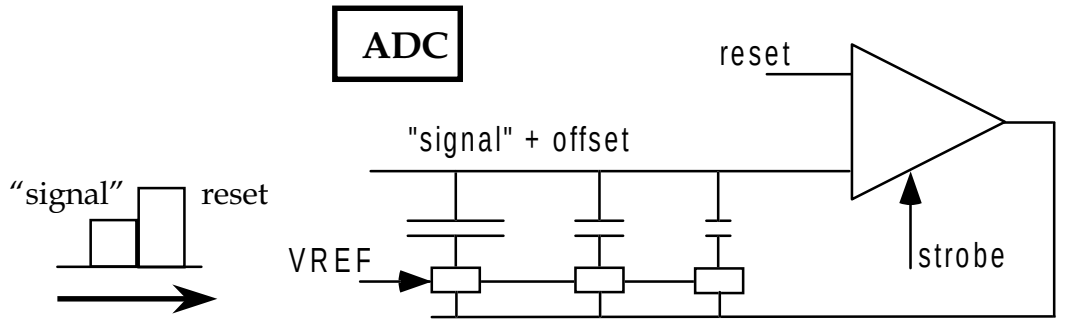


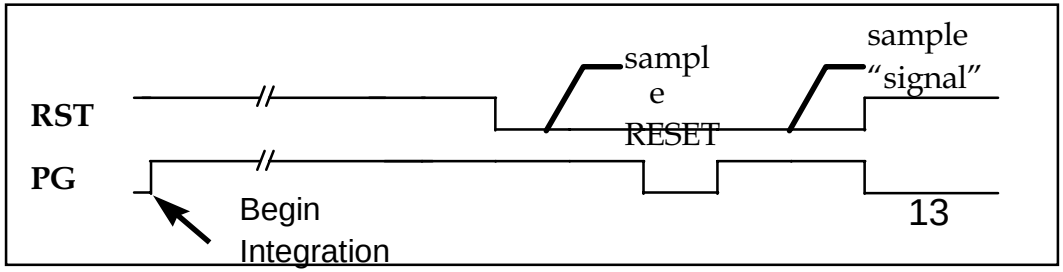
Signal Chain



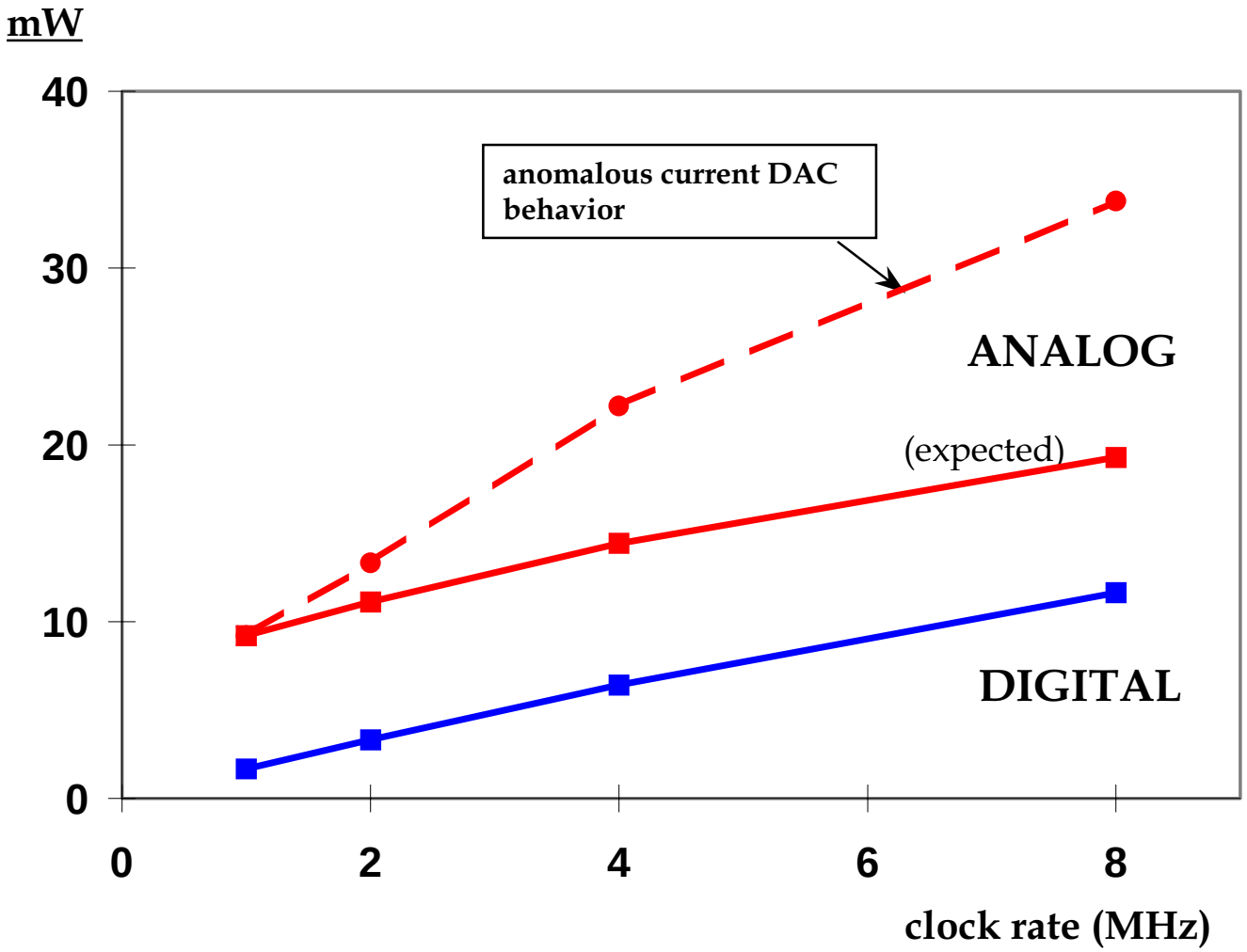
APS Photogate Pixel

ADC





ANALOG/DIGITAL POWER

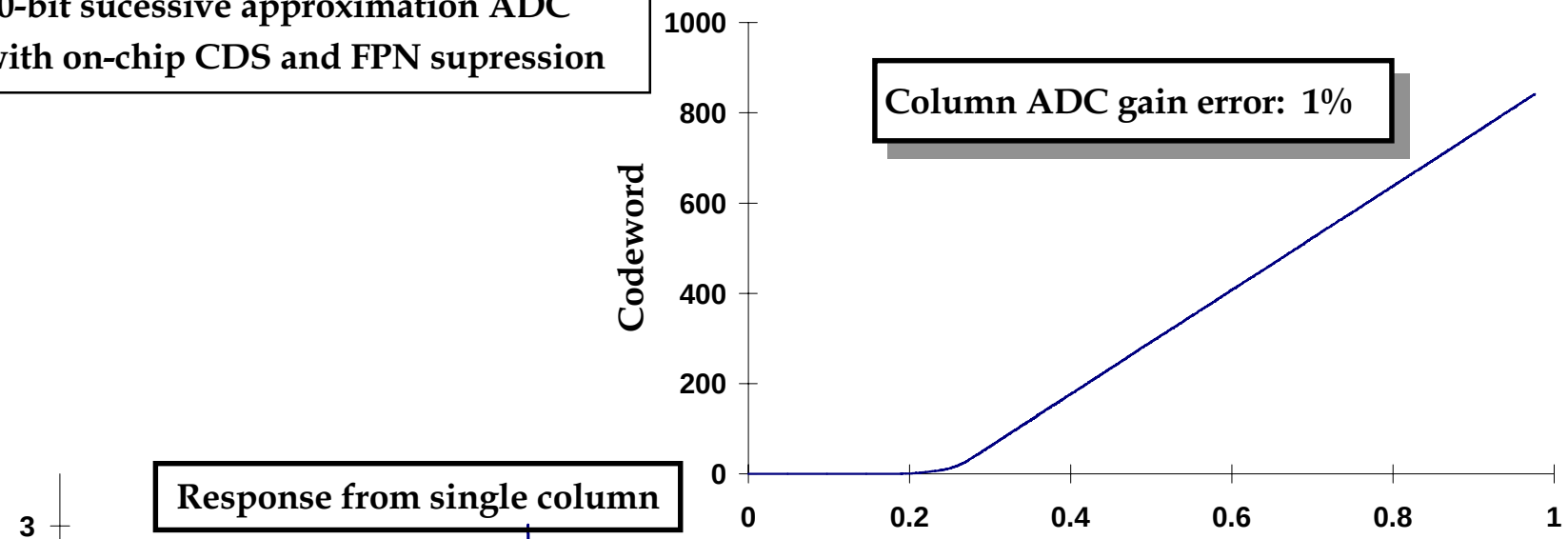


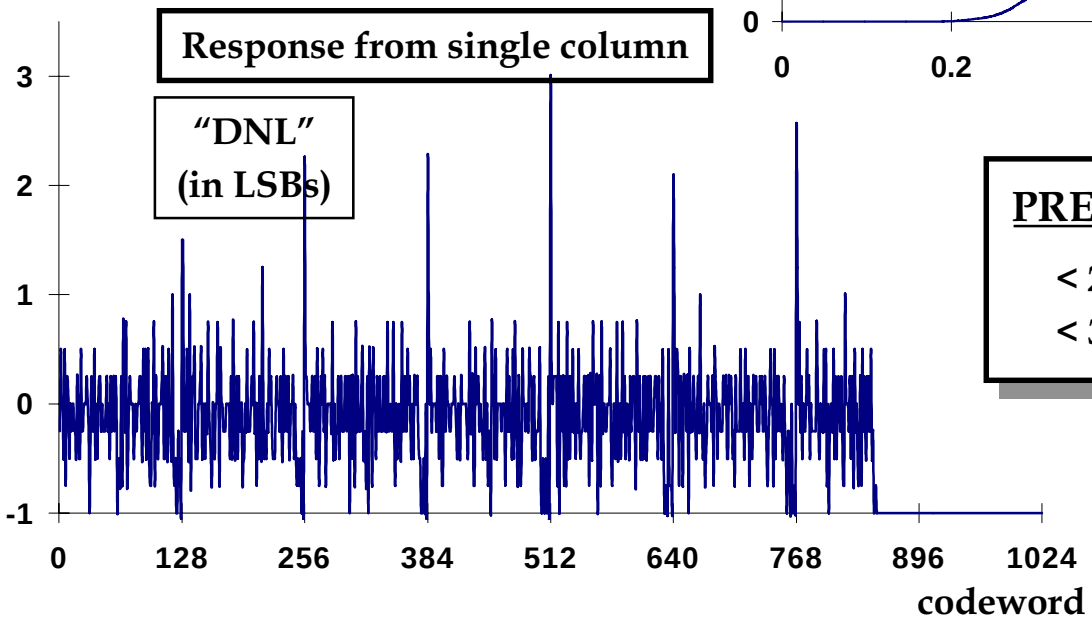
- **Voltage DAC: 4.6 mW**
- **Current DAC: 2.4 mW**

SH time = 70 msec
ADC conversion time = 60 msec
TX = 1 Volt
VLN: 5.5 mA
ADC Range: 3 V
10 bit serial output

256 COLUMN-PARALLEL ADCs

Binary Scaled Capacitor Array
10-bit sucessive approximation ADC
with on-chip CDS and FPN supression





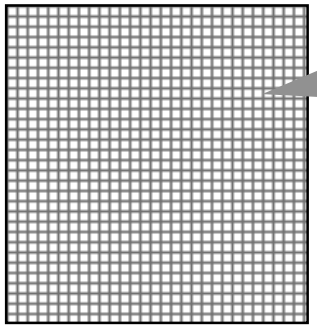
PRELIMINARY RESULTS

< 2 bits average DNL
< 3 bits worst case DNL

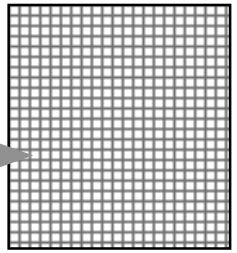
MULTI-FUNCTIONAL ONE-CHIP SMART SENSOR SYSTEM

smart sensors in a single-chip

- *high quality visible light imager*
- *On-chip image compression*
- *optical commuincation*
- *object recognition*
- *multiresolution*
- *optical navigation*

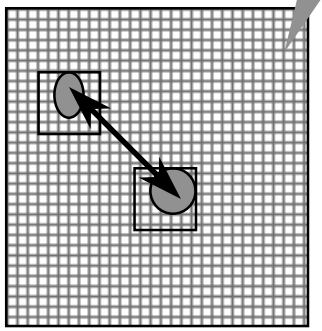


Large format, low power

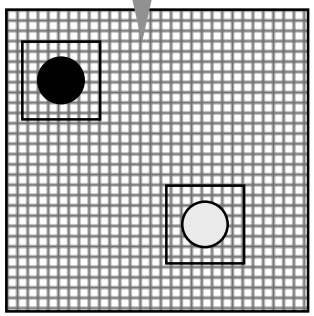


wavelet compression

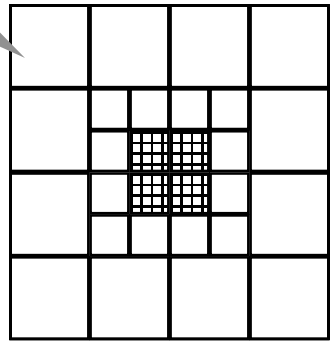
Content-based image compression



Auto-pointing and tracking
with centroid-on-chip



Navigation and guidance
with stars of different visual magnitudes



Multiresolution for
target tracking &
acquisition

ULTRA-HIGH FOV IMAGER

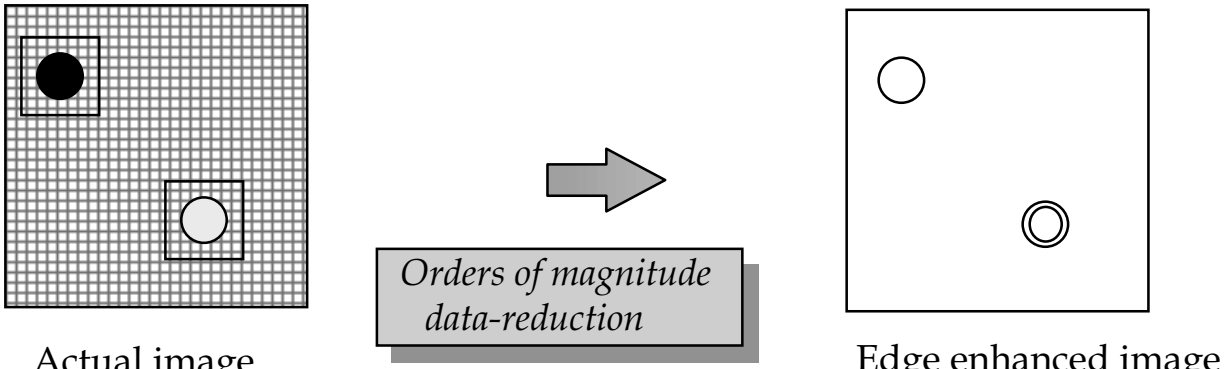
Rationale: Large format ultra-high FOV imager eliminates need for scanning

⇨ enables system miniaturization, vastly reduced system power

Great for surveillance purposes

Approach:

- Use wafer-scale integration to produce large-format 8Kx8K imager
- Use on-chip data reduction methods to ease off-chip communication bottleneck
  - On-chip DCT/wavelet based image compression scheme
  - On-chip motion detection
  - On-chip edge-detection: *adjacent pixel difference output; wavlet decompostion*



Actual image

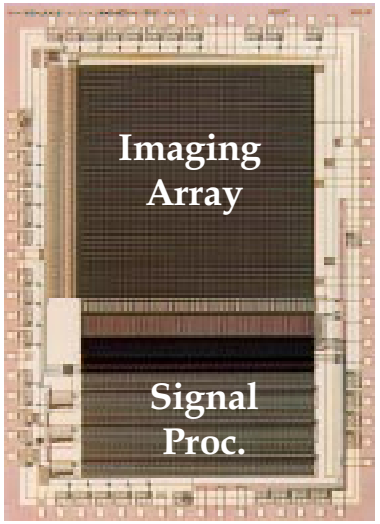
Edge enhanced image

ON-CHIP FOVEAL VISION

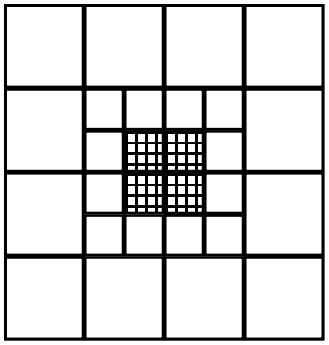
Rationale: Real-time multi-target acquisition and tracking
Autonomous navigation: nano-rovers and robots
Ultra-low multi-use sensor system

Approach:

- Develop on-chip programmable multi-resolution sensor by pixel averaging in column circuits to enable on-chip foveal vision
- Team with Amherst Systems for foveal vision system development
- On-chip fovea results in:
  - *100 x reduction in power*
  - *100x improvement in speed for real-time operation*
  - *10x reduction in mass and volume by eliminating off-chip processor and control*
- Large format imager helps in minimal motion of sensor head



Chip with commandable varying resolution



Multi-resolution enables real-time target acquisition

SUMMARY

- CMOS APS presents technology ideally suited for system-on-a-chip applications
- Enables sensor fusion by allowing parallel computing on digital imager data
- Enables on-sensor preprocessing for data-compression and data volume management
- Enables ultra-low power system without sacrificing imager quality
- APS on SOI technology needs to be demonstrated
- APS with low voltage power supply needs to be demonstrated